X20CM4323

Data sheet
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Translation of the original documentation

Publishing information

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Disclaimer

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1 General information

1.1 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual

1.2 Order data

Order number	Short description	Figure
	Other functions	
X20CM4323	X20 PWM module, 4 digital outputs for switching electro-mechanical loads, 24 VDC, oversampling output functions, time-triggered output functions, NetTime function	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 1: X20CM4323 - Order data

1.3 Module description

The module has digital outputs for connecting electromechanical loads (e.g. valves and relays) and additional functions such as edge generation.

Functions:

- Direct I/O
- Oversampled I/O
- PWM control
- Edge generator
- Error handling
- NetTime timestamp

Direct I/O

The module is equipped with 4 channels. "Direct I/O" makes it possible to use the physical I/Os like normal digital inputs and outputs.

Oversampled I/O

Identical to Direct I/O, only with the difference that the inputs or outputs can be read in or switched several times within one cycle. This allows higher frequency signals to be analyzed or output.

PWM

The module is equipped with 4 digital outputs with PWM functionality that can be used to control valves, for example.

Edge generator

The module is equipped with 4 edge generators that can be used to generate edges independently of the X2X cycle. The individual edges can be referenced to a timestamp or to other edges using an offset.

NetTime timestamp

An additional essential feature is the module's integrated timestamp function. This allows fast input edges such as registration marks to be detected independently of the system's X2X Link cycle time and provided with a precise input stamp. In the other direction, the module sets outputs at exactly specified times. This is done with a resolution up to 125 ns.

2 Technical description

2.1 Technical data

Order number	X20CM4323
Short description	
I/O module	4 digital outputs for switching electromechanical loads, pulse width modulation
General information	
B&R ID code	0xEC21
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Outputs	Yes, using LED status indicator and software (output error status)
Power consumption	
Bus	0.01 W
Internal I/O	1.4 W
External I/O	Corresponding to external load
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
UKCA	Yes
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
UL	cULus E115267 Industrial control equipment
Digital outputs	
Nominal voltage	24 VDC
Nominal output current	0.75 A
Total nominal current	3 A
Connection type	1-wire connections
Output circuit	Sink
Output protection	Thermal shutdown in the event of overcurrent or short circuit, integrated protection for switching inductive loads
Pulse width modulation	
Period duration	1 ms (1 kHz) or 20 µs (50 kHz)
Pulse duration	0 to 100%
Resolution for pulse duration	1%
Inrush current	1.5 A for max. 25 ms
Braking voltage when switching off inductive loads	27 VDC
Reverse polarity protection	No (must be protected externally)
Output voltage	
Minimum	18 VDC
Nominal	24 VDC
Maximum	48 VDC
Protective circuit	
External	24 VDC power supply - maximum current 10 A (melting fuse)
Electrical properties	
Electrical isolation	Bus isolated from channel and internal I/O power supply Channel not isolated from channel and internal I/O power supply
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	0 to 50°C
Vertical mounting orientation	0 to 40°C
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C

Table 2: X20CM4323 - Technical data

Order number	X20CM4323
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB12 separately. Order 1x bus module X20BM11 separately.
Pitch	12.5$^{+0.2}$ mm

Table 2: X20CM4323 - Technical data

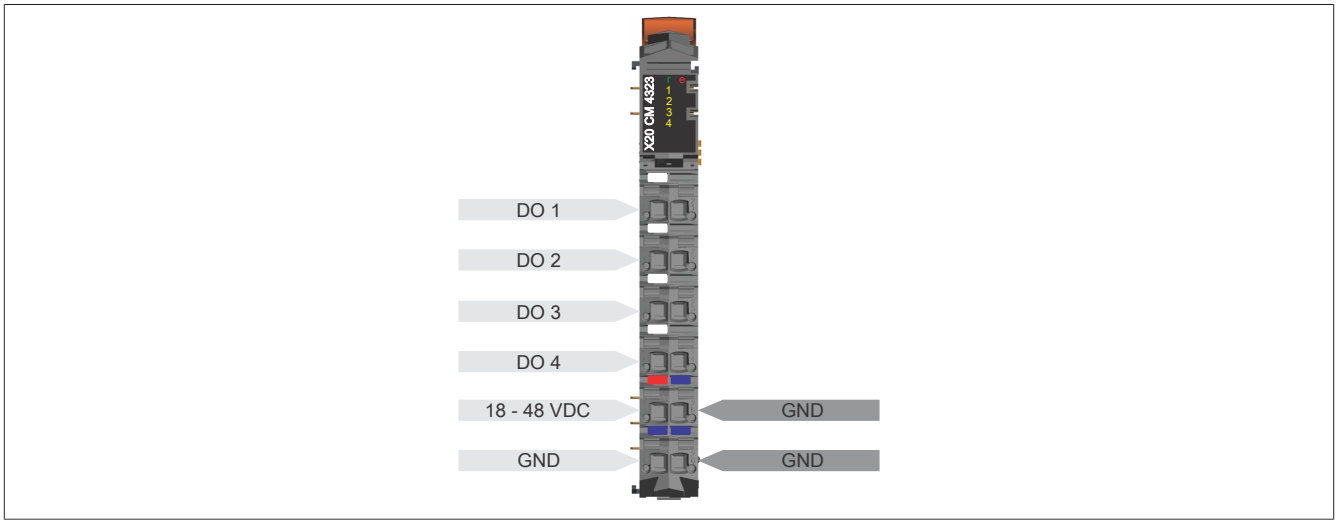
2.2 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

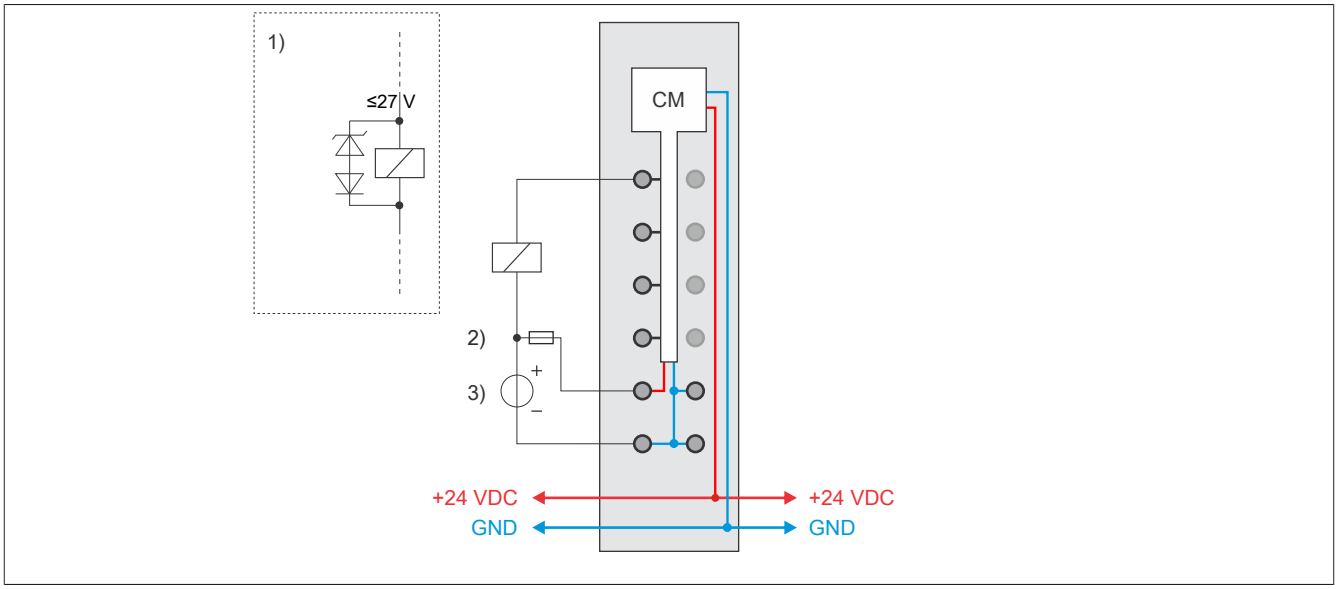
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Solid red / Single green flash		Invalid firmware
	1 - 4	Orange	On/Off	Status of the digital outputs
			Blinking	Short circuit / overcurrent cutoff
				Information: **The output is not automatically activated after an overcurrent cutoff. It must be switched on again.**

1) Depending on the configuration, a firmware update can take up to several minutes.

2.3 Pinout

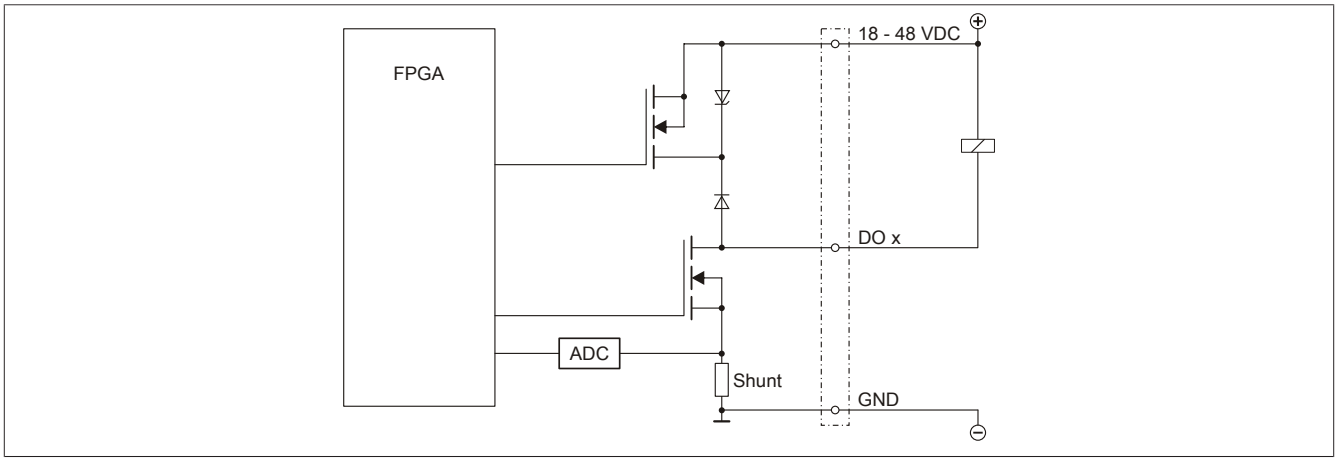


2.4 Connection example

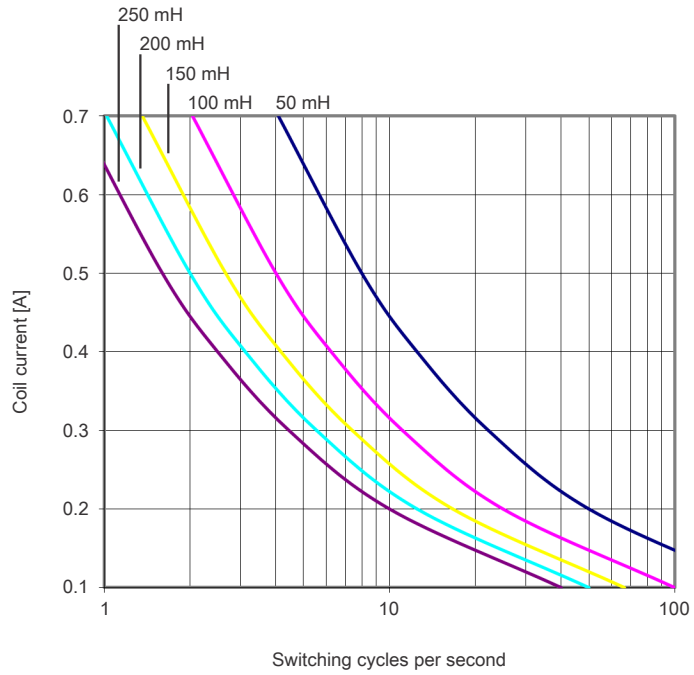


1) If larger inductances or more current should be handled, the "transil-diode combination" must be set externally on the relay/valve.
2) Fuse, 10 A slow-blow
3) Power supply 18 - 48 VDC

2.5 Output circuit diagram



2.6 Switching inductive loads



In principle, the inductance that is connected is limited by the maximum power dissipation of the module.

If larger inductances or more current are used, the "transil-diode combination" must be placed externally on the relay/valve (see "Connection example" on page 7).

Information:

The inductance of a relay/valve depends greatly on the core material being used. Therefore, an inductance must be used that corresponds to the diagram at 1Hz. This information can be found in the data sheet of the connected inductance (relay/valve).

3 Function description

3.1 System functions

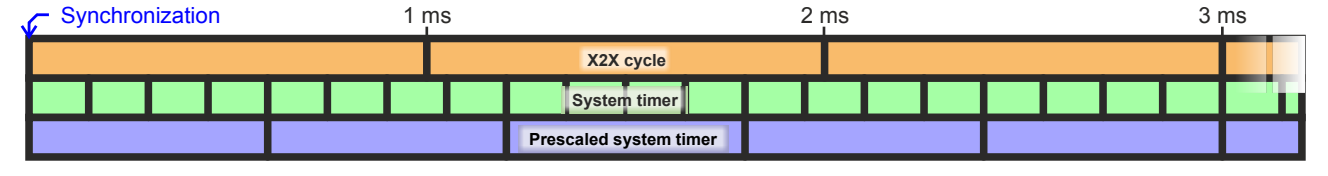
3.1.1 System timer

The module's individual functions all depend on a system timer. This internal "system cycle time" can be set from 25 to 255 µs. The functions can also be run using a configurable "prescaled system timer" to minimize the load on the module, thereby making it possible to use the shortest possible X2X cycle time.

The cycle of the prescaled system timer (and system timer) is referenced with the X2X Link as soon as the module has been started up and the X2X Link has been initialized. Since the system timer and the module's internal NetTime use the same timer, the two run synchronously from that point on. If the X2X cycle time is not a multiple of the system cycle time, there will be an offset; this can be calculated, however.

The following values apply to the following example:

X2X cycle	1 ms
System timer	150 µs
Prescaled system timer	4



Cycle prescaler

The "prescaled system timer" can be used as an alternative time source for the individual functions. This is useful if a function requires a very short system cycle. To reduce the module load in such a situation, other functions can be processed in a slower cycle.

3.1.2 Reference cycle

A reference cycle must be defined for data acquisition or transfer for oversampled I/Os and edge generation. At the beginning of each cycle, the acquired data is transferred as input or output data according to the respective function.

The following options are available as sources:

Source	Information
System timer	The value set in register "CfO_SystemCycleTime" is used as the reference cycle.
Prescaled system timer	The value set in register "CfO_SystemCyclePrescaler" is used as the reference cycle.
AOAI[1)]	The reference cycle is referenced with the AOAI interrupt of the X2X cycle.
SOSI[1)]	The reference cycle is referenced with the SOSI interrupt of the X2X cycle.

1) Cannot be used for edge generation.

Input data

- **Oversampled I/O**
  During each sample cycle, a bit from the output control buffers of the oversampled I/O channels is output to the configured physical output.

Output data

- **Oversampled I/O**
  - With relative addressing of the output control buffer, the new sample data is copied to an address relative to the output control buffer address current to the "reference cycle".
  - The reference cycle is also used to reference the sample cycle and thus the output data production and input data acquisition (e.g. to the X2X cycle).

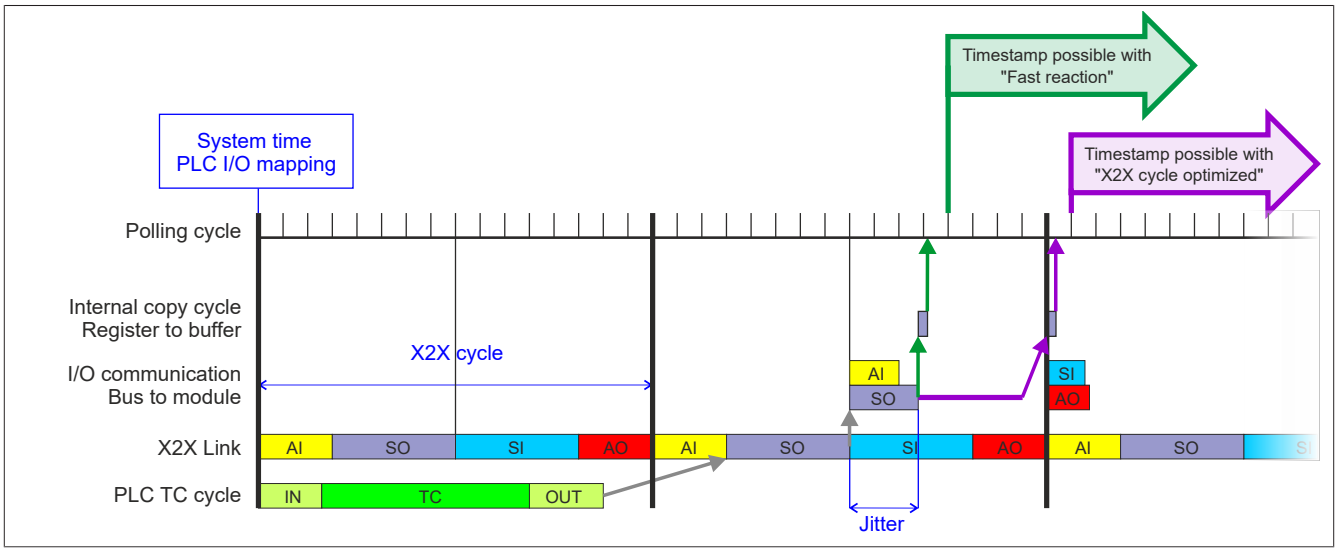
- **Edge generation**
  To ensure edge output with microsecond precision, edge generation is based on internal hardware components. One such comparator is available for one rising and one falling edge respectively for each physical output channel. The data for the comparators is prepared in "EdgeGenPollCycle". Therefore, a maximum of one rising and one falling edge can be generated for each physical output channel per "EdgeGenPollCycle". If timestamps are set that cannot be processed in time due to this limitation, then an EdgeGenWarning is generated. Processing of such timestamps is made up for as quickly as possible, as long as they are within EdgeGenUnitPickupDiff.
  The shorter this "generation cycle" is selected, the more negatively an enabled edge generator function affects the minimum X2X cycle time.

3.1.3 Edge generation

This register defines when the output data for the edge generation within the X2X cycle is applied.

Data type	Values	Information
USINT	10	"X2X cycle optimized" The data is applied permanently between the ASYNC IN (AI) and ASYNC OUT (AO) periods.
	15	"Fast reaction (jitter)" The data is applied immediately after SYNC OUT (SO) processing.

Setting "Fast reaction" results in jitter because the copy cycle of the SYNC OUT data can take different amounts of time. However, this only affects the moment at which the internal copy cycle takes place and therefore possibly also the earliest possible timestamp. Timestamps that are set outside of this jitter range are not affected by this.



3.1.4 Synchronization jitter

Since the controller that specifies the X2X NetTime and the module have different clocks, the module-internal X2X NetTime must be synchronized with the NetTime of the controller. Due to this synchronization, the module's internal X2X NetTime is corrected by a maximum of 1/8 µs per system cycle if necessary. This synchronization jitter becomes noticeable when using the NetTime with 1/8 µs resolution (max. ±1/8 µs).

If a 100% exact 1/8 µs resolution without jitter is required, then the "localtime 1/8 µs" must be used.

3.1.5 Use with Automation Studio

The module is supported via X2X and POWERLINK!

X2X Link supports the following synchronous cyclic data per module:

- 31 bytes of input data, consisting of 30 input bytes and an X2X status byte
- 30 bytes output data

To optimize use and prevent needless data transfer, data points can be adjusted as needed in Automation Studio. Unnecessary data points can be disabled, and the bit width of the data points can be defined.

3.2 Direct I/O

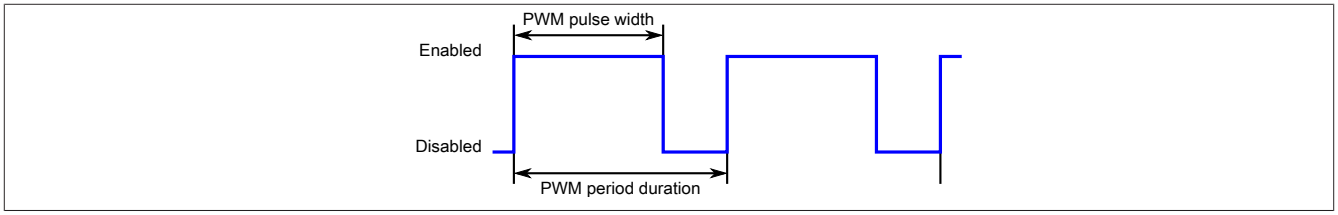
Direct I/O makes it possible to use the physical I/Os like normal I/Os. Additionally, the application can only set or reset I/Os (e.g. an output channel is set by the edge generator and manually reset by the application).

Information:

The registers are described in "Direct I/O" on page 28.

3.2.1 PWM

Pulse width modulation can also be set up using these registers. One of these registers is used to define the pulse width. At the beginning of each period, the output is switched on for the percentage of time set in this register.



3.3 Oversampled I/O

"Oversampled I/O" based on output control buffers. Output control occurs in one sample cycle (one sample cycle corresponds to one bit in the buffer).

In "Output control mode = single" every output buffer entry is marked as invalid once it has been executed. This ensures that the outputs are not supplied with invalid data. In this mode, the application needs to ensure that the module is always supplied with valid data.

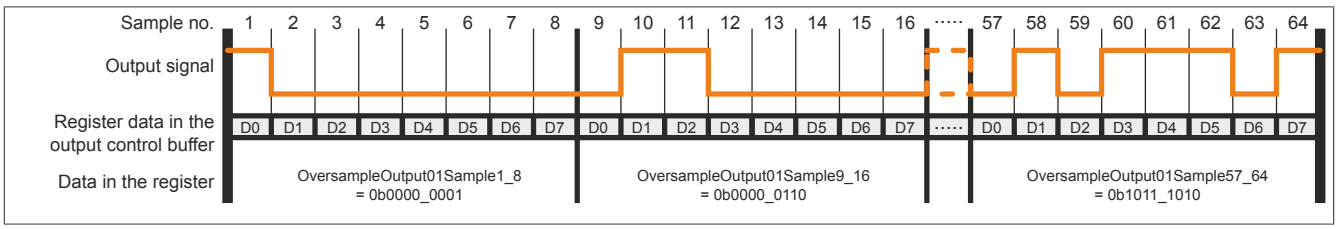
When using "Output control mode = continuous" the contents of the buffer are output again if the module is not supplied with new oversample output data.

3.3.1 Output data

Up to 64 samples (8 bytes) for each oversample I/O channel can be synchronously transferred with a X2X cycle. This data is copied to the specified address (absolute or relative) in the output control buffer at the set output copy cycle. 1 bit of this data is then output during each "sample cycle" to the physical output that is assigned to the oversample I/O channel.
Bit 0 of "OversampleOutputSample1_8" is copied to the output control buffer first, meaning that it is the first bit that is output. "OversampleOutputSample57_64" bit 7 is the last bit to be output.

Example

Assignment of "OversampleOutputSample" register data to the output signal:



Output operation

When "Output control mode = Single", every output buffer entry is marked as invalid once it has been executed. This ensures that the outputs are not supplied with invalid data. In this mode, the application needs to ensure that the module is always supplied with valid data.

When using "Output control mode = Continuous" the contents of the buffer are output again if the module is not supplied with new oversample output data.

Cyclic output control

If cyclic output control is enabled, then all data in the output control buffer is marked invalid as soon as it is output ("Output control mode = Single"). OutputControlError is generated if the module is not supplied with new data in time; in this case, a bit already output in the buffer would be output again. In this type of error situation, the output takes on the "Output default state" configured in register "CfO_Oversample-ConfigOutput".

If cyclic output control is disabled, then the data is output again if the output control buffer overflows ("Output control mode = Continuous").

Information:

All 256 bits of the output control buffer are always output.

Information:

The registers are described in "Oversampled I/O" on page 30.

3.3.2 Addressing the output control buffer

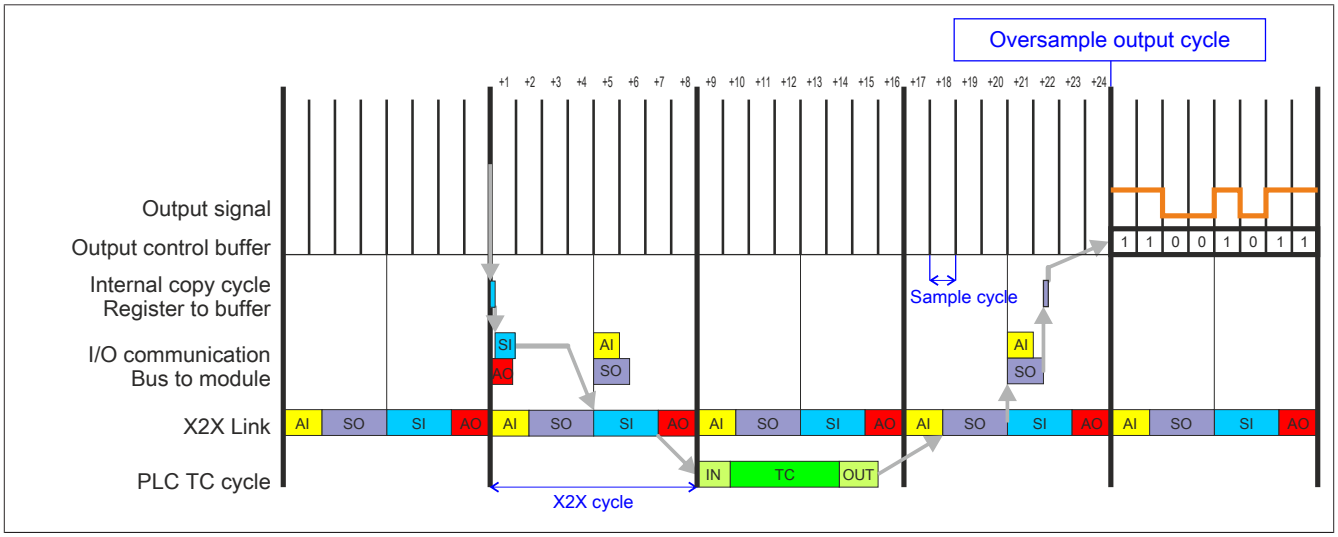
The module has one cyclic 256-bit output control buffer for each oversample channel. One bit is output from these buffers to the configured physical output channels in each "sample cycle". When new data is transferred to one of these buffers, the application must define where in the respective buffer the data should be written to. There are 2 possibilities available for this (absolute or relative "Output mode" in the Automation Studio I/O configuration).

3.3.3 Absolute addressing of the output control buffer

With absolute addressing, in each cycle where "OversampleOutputValidate = True", in addition to the oversample output sample data (in the "OversampleOutput0NSample" on page 32 registers) an address must also be transferred in the "OversampleOutputCycle" on page 32 register. This address determines where in the output control buffer the new data should be copied to. In order to calculate this address, the contents of register "OversampleInputCycle" on page 32, which contains the address of the most recently output data, and the transfer time to the module must be taken into consideration. To help avoid incorrect addressing of the output control buffer, the buffer section that is capable of being written to can be limited using register "OversampleOutputWindow" on page 31. This window will always be shifted relative to the current sample address. An "OutputCopyError" will be triggered if an attempt is made to write to an address that is outside of this window.

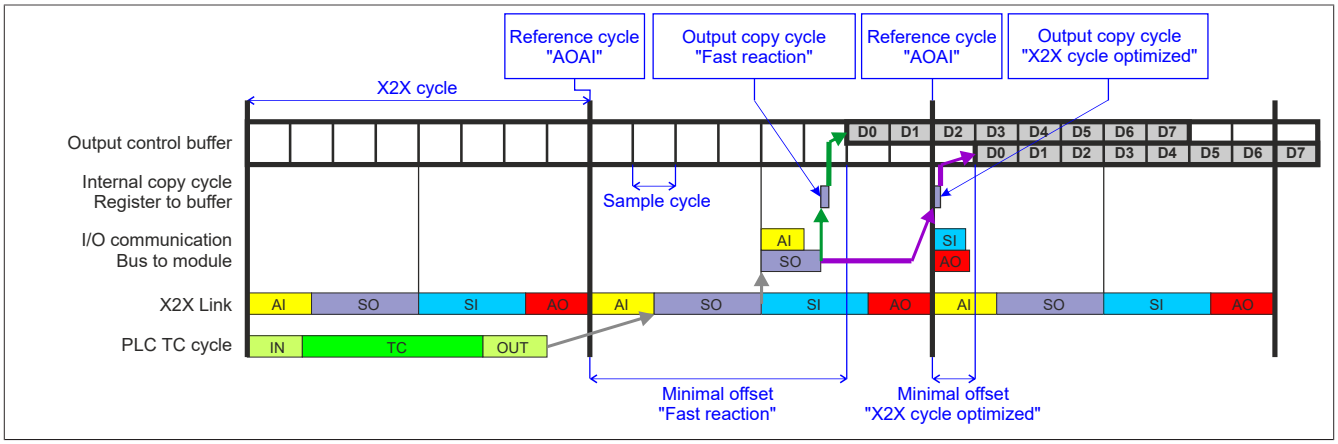
Example

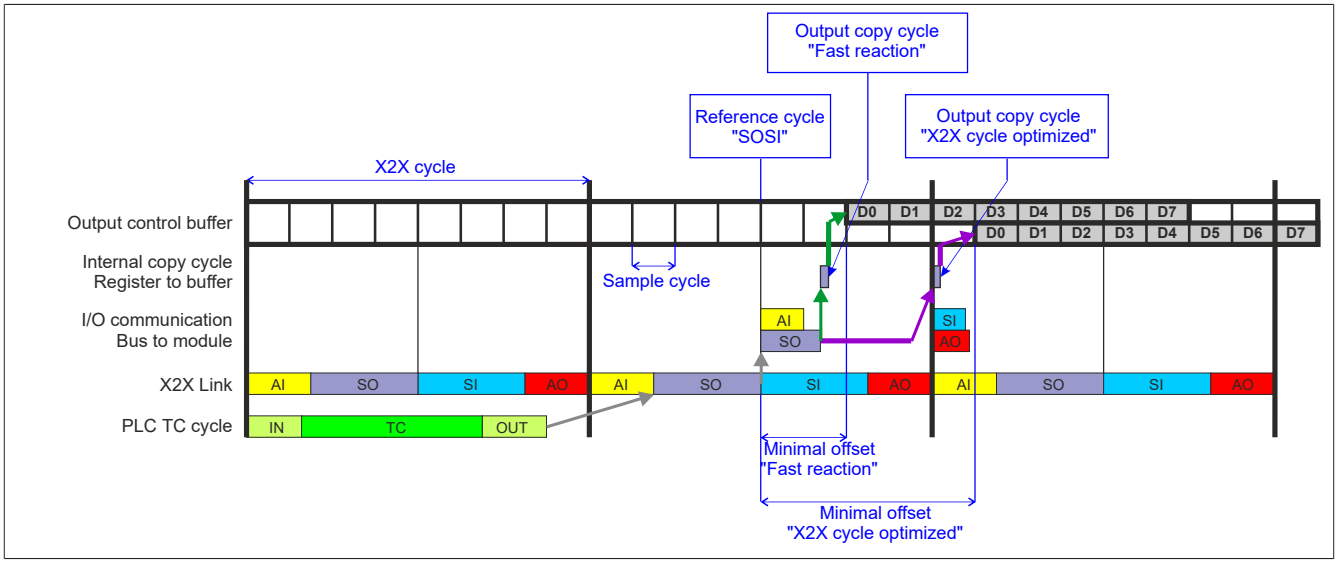
Timing of an oversample output cycle in absolute output mode ("SI frame generation = Fast reaction", "Output copy cycle = Fast reaction", 8 samples per X2X cycle):



3.3.4 Relative addressing of the output control buffer

When "OversampleOutputValidate = True", then the oversample output sample data is automatically copied to an address relative to the last referenced address at the defined output copy cycle time. The "OversampleSampleOffset" on page 32 register serves as the offset. The new data cannot start being output immediately at the output copy cycle time because it takes time to copy the data from the registers to the buffer. This means that an offset of 0 is not allowed. The relative output control buffer address + offset must point to an address within the "oversample output window". The oversample output window is always offset relative to the current sample address. An OutputCopyError is triggered if an attempt is made to write to an address that is outside of this window.





3.4 PWM control

The module is equipped with digital outputs for switching electromechanical loads (e.g. valves and relays) and additional functions, e.g. edge generation.

With a resolution down to 125 ns, the module makes it possible to set switching operations at precisely specified times.

The following operating modes can optionally be supplemented with PWM functionality:

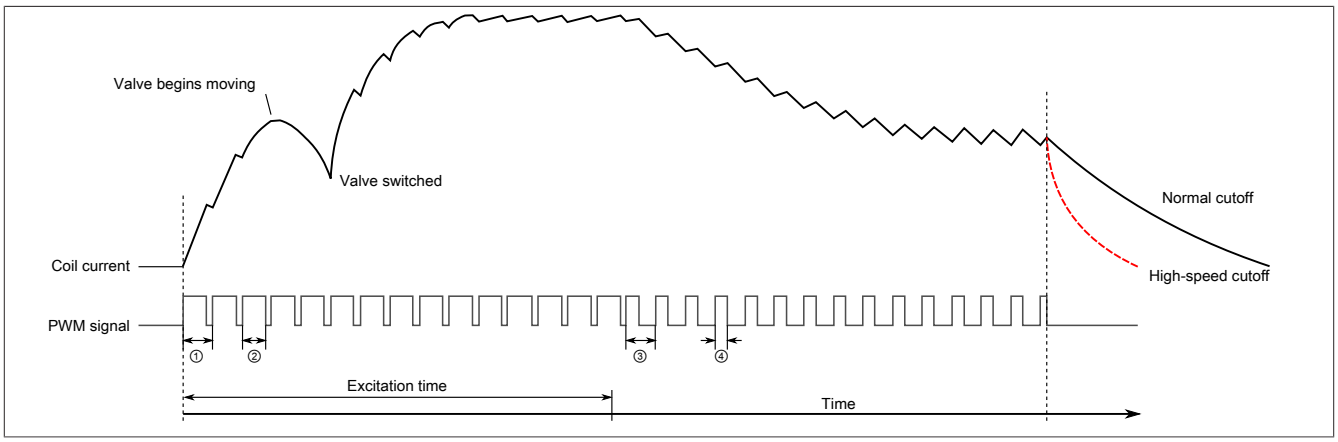
- Direct I/O
- Oversampled I/O
- Edge generator
- Edge generator in toggle operation for output patterns such as digital cam switches (e.g. digital cam switch of function block "ASMcDcsTimedDigitalCamSwitch")

Additional functions:

- PWM modulation of outputs for setting the overexcitation and holding current.
- Configuration of each channel by specifying the PWM period duration
- Control value for overexcitation and holding current as well as the overexcitation time
- Possibility of disabling the high-speed cutoff

Example

The following graphic shows the correlation between the individual PWM switching phases and the coil behavior of a valve.



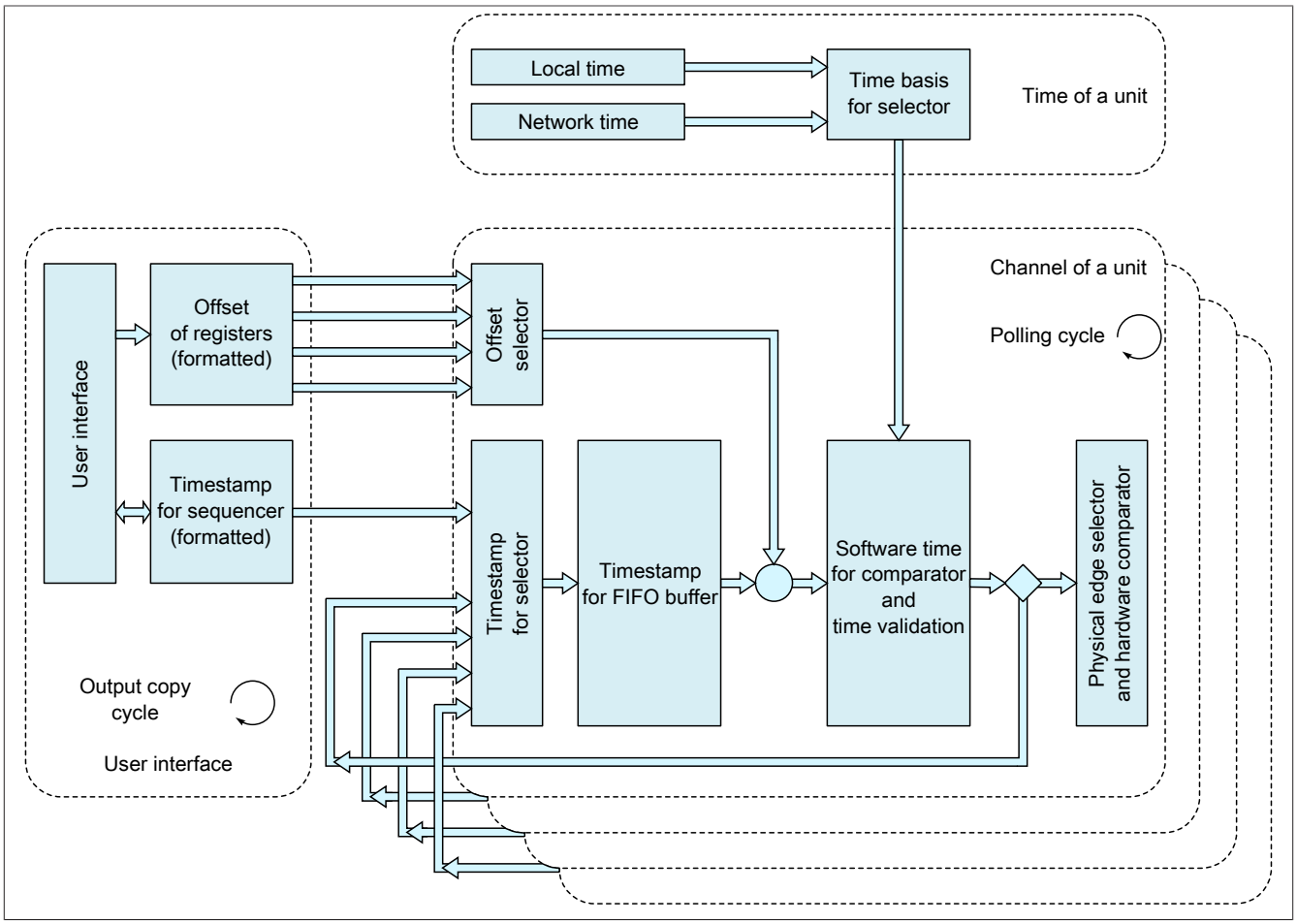
①,③ PWM period duration
② PWM excitation current value
④ PWM holding current value

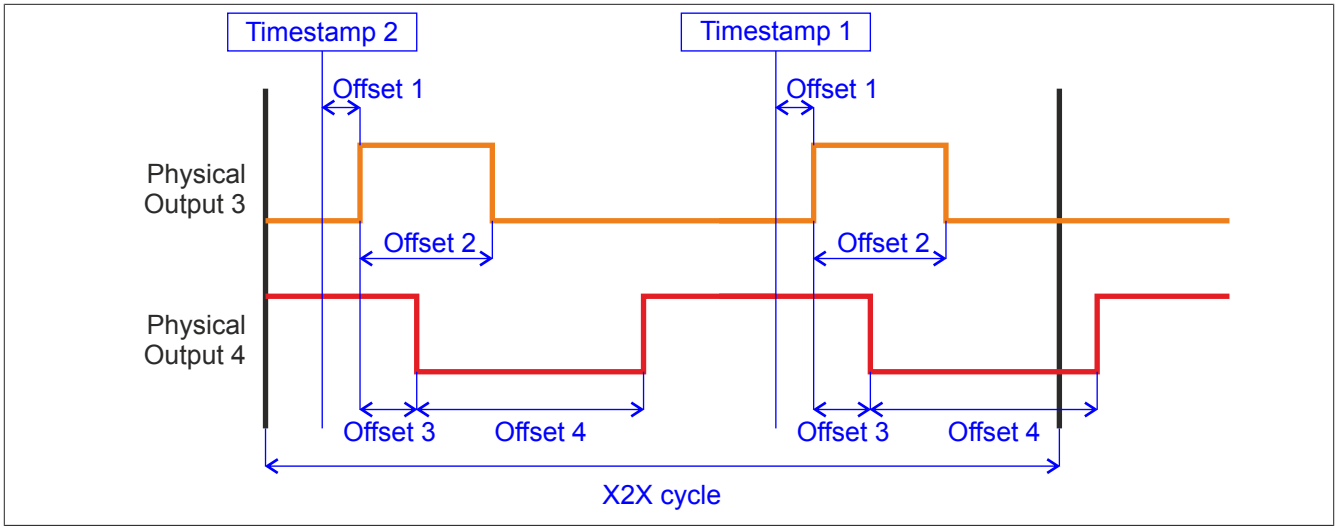
Information:

The registers are described in "PWM" on page 33.

3.5 Edge generator

The edge generator is based on 4 units. The units are able to generate edges independently of the X2X cycle. For each unit, up to 4 timestamps can be set per X2X cycle. The individual edges can then be referenced to this timestamp or to other edges using an offset.





Information:

The registers are described in "Edge generator" on page 34.

3.5.1 Mode "DigitalCamSwitch"

"Unit 0x" in Automation Studio I/O configuration.

Mode "DigitalCamSwitch" can also be selected for the configuration of the edge generator in Automation Studio for each unit.
In this mode, the entire configuration and operation is carried out exclusively via the function blocks of motion library "ASMcDcs". For additional information, see the corresponding ASMcDcs function block descriptions.

3.5.2 Ring-shaped interlinking of edges

If individual edges are linked together in a ring (e.g. edge 2 is relative to edge 1 and edge 1 is relative to edge 2), a header for the ring must be defined via bit 11 "Ring-shaped interlinking" so that such a cycle starts without a timestamp. In Automation Studio, bit 11 "Ring-shaped interlinking" is set by default in all units for edge 1. If such a ring is branched (e.g. a third edge is relative to an edge within the ring), it is important to ensure that the internal FIFO buffer that is available to each physical I/O edge is not overfilled. This happens if more than 12 edges are generated by the ring, but these should only be output in the future. If this situation occurs, where a ring generates edges even though the FIFO buffer is full, EdgeGenError is triggered.

3.5.3 Offset formats

Automation Studio provides 3 different parameters for setting offsets.

- **Offset format:** This parameter makes it possible to select the file type (16-bit or 32-bit) for cyclic transfer and only affects"EdgeGenOffset" on page 37 registers.
  Acyclic transfer of offset values with register "CfO_EdgeGenOffset_32bit" on page 37 is not affected by this and always remains 32 bits wide.
- **Offset 01 to Offset 04:** These parameters have 2 possible settings:
  - Initial configuration: The offset value is only written once during configuration.
  - Cyclic data: A data point is created in the Automation Studio I/O mapping and the offset value is written cyclically.
- **Offset 01 value to Offset 04 value:** The actual offset value.

3.5.4 Using timestamps

Transferring timestamps

Up to 4 timestamp elements can be transferred per X2X cycle.

If new timestamp data should be applied to the module, then the sequence number must be increased by the number of timestamp elements to be applied. If several elements are transferred within an X2X cycle, it must also be ensured that the individual timestamps are transferred to the buffer in the order in which they follow each other.

Depending on how much the sequence number is increased, 1 to 4 of these timestamp elements are transferred to the buffer. If an attempt is made to set a timestamp to a time that has already expired, EdgeGenWarning is generated.

If no more new timestamp data can be recorded by the module (e.g. because the maximum number of timestamps has been reached), the last sequence recorded by the module can be read out.

Edge resolution

Edges can be resolved with an accuracy of 1 µs or 1/8 µs. If "Timestamp resolution = 1/8 µs" is used, it is important to ensure that the timestamp data also has a resolution of 1/8 µs. Since both the controller system time and X2X NetTime only resolve down to the microsecond, the system time or NetTime must be shifted 3 bits to the left or multiplied by 8 in the application. This value can then be used as reference for timestamps with a resolution of 1/8 µs. It is also possible to use 1/8 µs timestamps from input edges as a reference.

When using the NetTime with 1/8 µs resolution, the synchronization jitter affects the output results (see "Synchronization jitter" on page 10).

Processing timestamps

Up to 12 timestamps can be transferred to a buffer for future processing. The timestamps must be transferred to the buffer in the order in which they should be output. It is therefore not possible to set a timestamp in the future and then set a timestamp that is earlier than the one transferred first.

If a timestamp is already in the past at the start of processing, a time difference can be specified up to which the processing of the timestamp can still be made up. Timestamps in the past are processed as quickly as possible as long as they are within the specified catch-up difference. EdgeGenWarning is triggered as soon as a timestamp could not be processed in time and had to be "caught up". If a timestamp could not be caught up because it is outside the catch-up difference, "EdgeGenError" results in addition to the "EdgeGenWarning".

3.6 Error handling

If one of the functions detects an error, then an error bit is set in one of the error state registers. The application is now able to react to this and acknowledge the errors by setting a respective bit in the "Acknowledge error messages" registers. This resets the bit in the error status register. If the error source persists, then the error bit is set again as soon as the error is detected again (i.e. resetting is not possible).

After the error source has been corrected and the error acknowledged, the module must be re-enabled by disabling and re-enabling the enable registers in order to resume processing. The following registers are affected:

- Oversampling configuration: Register "OversampleEnable" on page 32
- Edge generation - Enabling units: Register "EdgeGenEnable" on page 36
- Enabling the PWM function: Register "DigitalOutputEnable" on page 29

If an error occurs (not a warning), this is indicated by the red "e" LED on the module (double flash). This signal is automatically acknowledged as soon as the source of the error has been corrected.

Information:

The registers are described in "Error handling" on page 25.

3.7 NetTime Technology

NetTime refers to the ability to precisely synchronize and transfer system times between individual components of the controller or network (controller, I/O modules, X2X Link, POWERLINK, etc.).

This allows the moment that events occur to be determined system-wide with microsecond precision. Upcoming events can also be executed precisely at a specified moment.

3.7.1 Time information

Various time information is available in the controller or on the network:

- System time (on the PLC, Automation PC, etc.)
- X2X Link time (for each X2X Link network)
- POWERLINK time (for each POWERLINK network)
- Time data points of I/O modules

The NetTime is based on 32-bit counters, which are increased with microsecond resolution. The sign of the time information changes after 35 min, 47 s, 483 ms and 648 µs; an overflow occurs after 71 min, 34 s, 967 ms and 296 µs.

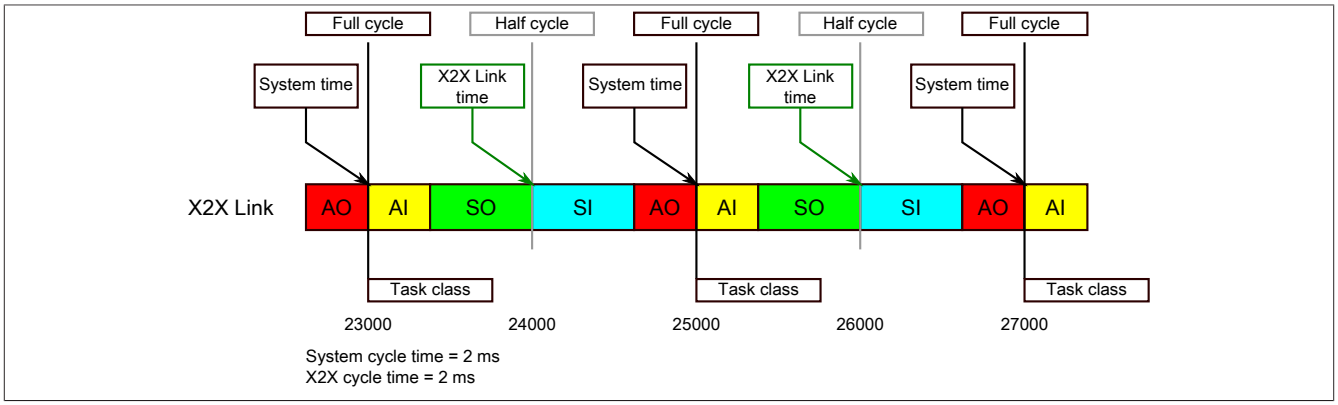
The initialization of the times is based on the system time during the startup of the X2X Link, the I/O modules or the POWERLINK interface.

Current time information in the application can also be determined via library AsIOTime.

3.7.1.1 Controller data points

The NetTime I/O data points of the controller are latched to each system clock and made available.

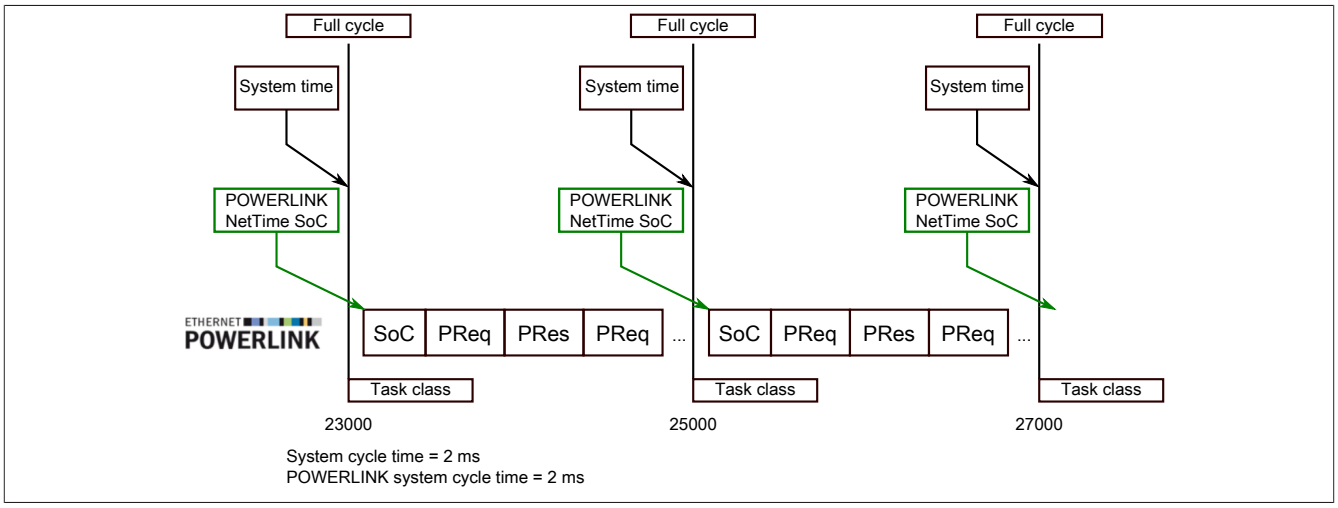
3.7.1.2 X2X Link - Reference time point



The reference time point on the X2X Link network is always calculated at the half cycle of the X2X Link cycle. This results in a difference between the system time and the X2X Link reference time point when the reference time is read out.

In the example above, this results in a difference of 1 ms, i.e. if the system time and X2X Link reference time are compared at time 25000 in the task, then the system time returns the value 25000 and the X2X Link reference time returns the value 24000.

3.7.1.3 POWERLINK - Reference time point

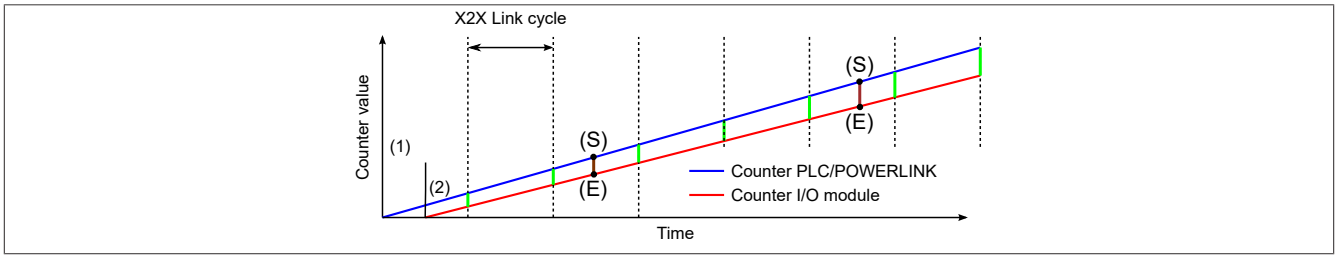


The POWERLINK reference time point is always calculated at the start of cycle (SoC) of the POWERLINK network. The SoC starts 20 µs after the system clock due to the system. This results in the following difference between the system time and the POWERLINK reference time:

POWERLINK reference time = System time - POWERLINK cycle time + 20 µs

In the example above, this means a difference of 1980 µs, i.e. if the system time and POWERLINK reference time are compared at time 25000 in the task, then the system time returns the value 25000 and the POWERLINK reference time returns the value 23020.

3.7.1.4 Synchronization of system time/POWERLINK time and I/O module



At startup, the internal counters for the controller/POWERLINK (1) and the I/O module (2) start at different times and increase the values with microsecond resolution.

At the beginning of each X2X Link cycle, the controller or POWERLINK network sends time information to the I/O module. The I/O module compares this time information with the module's internal time and forms a difference (green line) between the two times and stores it.

When a NetTime event (E) occurs, the internal module time is read out and corrected with the stored difference value (brown line). This means that the exact system moment (S) of an event can always be determined, even if the counters are not absolutely synchronous.

Note

The deviation from the clock signal is strongly exaggerated in the picture as a red line.

3.7.2 Timestamp functions

NetTime-capable modules provide various timestamp functions depending on the scope of functions. If a timestamp event occurs, the module immediately saves the current NetTime. After the respective data is transferred to the controller, including this precise moment, the controller can then evaluate the data using its own NetTime (or system time), if necessary.
For details, see the respective module documentation.

3.7.2.1 Time-based inputs

NetTime Technology can be used to determine the exact moment of a rising edge at an input. The rising and falling edges can also be detected and the duration between 2 events can be determined.

Information:

The determined moment always lies in the past.

3.7.2.2 Time-based outputs

NetTime Technology can be used to specify the exact moment of a rising edge on an output. The rising and falling edges can also be specified and a pulse pattern generated from them.

Information:

The specified time must always be in the future, and the set X2X Link cycle time must be taken into account for the definition of the moment.

3.7.2.3 Time-based measurements

NetTime Technology can be used to determine the exact moment of a measurement that has taken place. Both the starting and end moment of the measurement can be transmitted.

4 Register description

4.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 System user's manual.

4.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration - General						
513	CfO_SlframeGenID	USINT				•
Configuration - System timer						
642	CfO_SystemCycleTime	UINT				•
646	CfO_SystemCycleOffset	INT				•
650	CfO_SystemCyclePrescaler	UINT				•
Configuration - Direct I/O						
899	CfO_DirectIOClearMask0_3	USINT				•
903	CfO_DirectIOSetMask0_3	USINT				•
905	CfO_OutputUpdateCycle	USINT				•
Configuration - Oversampled I/O						
1025	CfO_OversampleMode	USINT				•
1027	CfO_OversampleSampleCycleID	USINT				•
1029	CfO_OversampleRelativeCycleID	USINT				•
1031	CfO_OversampleConsumeCycleID	USINT				•
1033	CfO_OversampleOutputBits	USINT				•
1037	CfO_OversampleOutputWindow	USINT				•
1049 + (N*2)	CfO_OversampleConfigOutputN (index N = 0 to 3)	USINT				•
Configuration - PWM						
1282 + (N-1) * 32	CfO_PWM0N_Periode (index N = 1 to 4)	UINT				•
1286 + (N-1) * 32	CfO_PWM0N_Duty1 (index N = 1 to 4)	UINT				•
1290 + (N-1) * 32	CfO_PWM0N_Duty2 (index N = 1 to 4)	UINT				•
1294 + (N-1) * 32	CfO_PWM0N_Duty1Time (index N = 1 to 4)	UINT				•
1298 + (N-1) * 32	CfO_PWM0N_Duty1TimeBase (index N = 1 to 4)	UINT				•
1302 + (N-1) * 32	CfO_PWM0N_FastSwitchOff (index N = 1 to 4)	UINT				•
1409	CfO_PWM_UpdateCycle	USINT				•
Configuration - Edge generator						
2945	CfO_EdgeGenPollCycleEventID	USINT				•
2947	CfO_EdgeGenConsumeCycleEventID	USINT				•
3585 + (N-1) * 64	CfO_EdgeGenUnit0NMode (index N = 1 to 4)	USINT				•
3589 + (N-1) * 64	CfO_EdgeGenUnit0NTimestampFifoLim (index N = 1 to 4)	USINT				•
3591 + (N-1) * 64	CfO_EdgeGenUnit0NTimestampRegCount (index N = 1 to 4)	USINT				•
3596 + (N-1) * 64	CfO_EdgeGenUnit0NPickupDiff (index N = 1 to 4)	UDINT				•
3602 + (N-1) * 64	CfO_EdgeGenUnit0NConfigEdge0 (index N = 1 to 4)	UINT				•
3606 + (N-1) * 64	CfO_EdgeGenUnit0NConfigEdge1 (index N = 1 to 4)	UINT				•
3610 + (N-1) * 64	CfO_EdgeGenUnit0NConfigEdge2 (index N = 1 to 4)	UINT				•
3614 + (N-1) * 64	CfO_EdgeGenUnit0NConfigEdge3 (index N = 1 to 4)	UINT				•
Communication - General						
546	ProtocolError (16-bit)	UINT	•			
547	ProtocolError (8-bit)	USINT	•			
550	ProtocolSequenceViolation (16-bit)	UINT	•			

Register description

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
551	ProtocolSequenceViolation (8-bit)	USINT	•			
Communication - Error register						
257	Error status - Output data	USINT	•			
	OutputControlError	Bit 4				
	OutputCopyError	Bit 5				
259	Error messages - Edge generator	USINT	•			
	EdgeGen01Error	Bit 0				
	EdgeGen01Warning	Bit 1				
	EdgeGen02Error	Bit 2				
	EdgeGen02Warning	Bit 3				
	EdgeGen03Error	Bit 4				
	EdgeGen03Warning	Bit 5				
	EdgeGen04Error	Bit 6				
	EdgeGen04Warning	Bit 7				
321	Acknowledge error messages - Output data	USINT			•	
	QuitOutputControlError	Bit 4				
	QuitOutputCopyError	Bit 5				
323	Acknowledge error messages - Edge generator	USINT			•	
	QuitEdgeGen01Error	Bit 0				
	QuitEdgeGen01Warning	Bit 1				
	QuitEdgeGen02Error	Bit 2				
	QuitEdgeGen02Warning	Bit 3				
	QuitEdgeGen03Error	Bit 4				
	QuitEdgeGen03Warning	Bit 5				
	QuitEdgeGen04Error	Bit 6				
	QuitEdgeGen04Warning	Bit 7				
1443	Error status - Overcurrent of a PWM output	USINT	•			
	DigitalOutput01Err	BOOL				
	DigitalOutput02Err	BOOL				
	DigitalOutput03Err	BOOL				
	DigitalOutput04Err	BOOL				
1463	Acknowledge error messages - Overcurrent of a PWM output	USINT			•	
	DigitalOutput01ErrQuit	BOOL				
	DigitalOutput02ErrQuit	BOOL				
	DigitalOutput03ErrQuit	BOOL				
	DigitalOutput04ErrQuit	BOOL				
Communication - System timer						
683	SDCLifeCount	SINT	•			
Communication - Direct I/O						
915	Direct operation of the output channel - Output status	USINT			•	
	DigitalOutput01	Bit 0				
	DigitalOutput02	Bit 1				
	DigitalOutput03	Bit 2				
	DigitalOutput04	Bit 3				
1459	Direct operation of the output channel - Enabling the PWM function	USINT			•	
	DigitalOutput01Enable	Bit 0				
	DigitalOutput02Enable	Bit 1				
	DigitalOutput03Enable	Bit 2				
	DigitalOutput04Enable	Bit 3				
1466 + (N-1) * 4	PwmPeriode0N (index N = 1 to 4)	UINT			•	
1482 + (N-1) * 4	PwmDuty0N (index N = 1 to 4)	UINT			•	
Communication - Oversampled I/O (output)						
1079	OversampleInputCycle	USINT	•			
1059	Oversampling configuration	USINT			•	
	OversampleEnable	Bit 1				
	OversampleOutputValidate	Bit 2				
1063	OversampleOutputCycle	USINT			•	
	OversampleSampleOffset	USINT			•	
1088 + N	OversampleOutput0NSample1_8 (index N = 1 to 4)	USINT			•	
1092 + N	OversampleOutput0NSample9_16 (index N = 1 to 4)	USINT			•	
1096 + N	OversampleOutput0NSample17_24 (index N = 1 to 4)	USINT			•	
1100 + N	OversampleOutput0NSample25_32 (index N = 1 to 4)	USINT			•	
1104 + N	OversampleOutput0NSample33_40 (index N = 1 to 4)	USINT			•	
1108 + N	OversampleOutput0NSample41_48 (index N = 1 to 4)	USINT			•	
1112 + N	OversampleOutput0NSample49_56 (index N = 1 to 4)	USINT			•	
1116 + N	OversampleOutput0NSample57_64 (index N = 1 to 4)	USINT			•	
Communication - Edge generator						
6145 + (N-1) * 256	Enabling units	USINT			•	
	EdgeGen0NEnable EdgeGen0NEnableReadback (index N = 1 to 4)	Bit 0				

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
6147 + (N-1) * 256	EdgeGen0NSequence	USINT			•	
	EdgeGen0NSequenceReadback	USINT	•			
6180 + (N-1) * 256	EdgeGen0NOffset1 (index N = 1 to 4) (32-bit) CfO_EdgeGen0NOffset_32bit1 (index N = 1 to 4)	UDINT			•	•
6182 + (N-1) * 256	EdgeGen0NOffset1 (index N = 1 to 4) (16-bit)	UINT			•	
6188 + (N-1) * 256	EdgeGen0NOffset2 (index N = 1 to 4) (32-bit) CfO_EdgeGen0NOffset_32bit2 (index N = 1 to 4)	UDINT			•	•
6190 + (N-1) * 256	EdgeGen0NOffset2 (index N = 1 to 4) (16-bit)	UINT			•	
6196 + (N-1) * 256	EdgeGen0NOffset3 (index N = 1 to 4) (32-bit) CfO_EdgeGen0NOffset_32bit3 (index N = 1 to 4)	UDINT			•	•
6198 + (N-1) * 256	EdgeGen0NOffset3 (index N = 1 to 4) (16-bit)	UINT			•	
6204 + (N-1) * 256	EdgeGen0NOffset4 (index N = 1 to 4) (32-bit) CfO_EdgeGen0NOffset_32bit4 (index N = 1 to 4)	UDINT			•	•
6206 + (N-1) * 256	EdgeGen0NOffset4 (index N = 1 to 4) (16-bit)	UINT			•	
6212 + (N-1) * 256	EdgeGen0NTimestamp1 (index N = 1 to 4) (32-bit)	UDINT			•	
6214 + (N-1) * 256	EdgeGen0NTimestamp1 (index N = 1 to 4) (16-bit)	UINT			•	
6220 + (N-1) * 256	EdgeGen0NTimestamp2 (index N = 1 to 4) (32-bit)	UDINT			•	
6222 + (N-1) * 256	EdgeGen0NTimestamp2 (index N = 1 to 4) (16-bit)	UINT			•	
6228 + (N-1) * 256	EdgeGen0NTimestamp3 (index N = 1 to 4) (32-bit)	UDINT			•	
6230 + (N-1) * 256	EdgeGen0NTimestamp3 (index N = 1 to 4) (16-bit)	UINT			•	
6236 + (N-1) * 256	EdgeGen0NTimestamp4 (index N = 1 to 4) (32-bit)	UDINT			•	
6238 + (N-1) * 256	EdgeGen0NTimestamp4 (index N = 1 to 4) (16-bit)	UINT			•	

4.3 General registers

4.3.1 Defining the moment for generating synchronous input data

Name:
CfO_SIframeGenID
"SI frame generation" in the Automation Studio I/O configuration.

When the synchronous input data is generated for transfer is defined in this register.

Data type	Values	Information
USINT	9	X2X cycle optimized
	14	Fast reaction

4.3.2 Number of X2X protocol errors

Name:
ProtocolError

This register contains an error counter that specifies the number of X2X protocol errors. In the I/O configuration, parameter "Network information" can be used to help configure a data point for this register with a bit width of 8 or 16 bits in the I/O mapping.

Data type	Values	Information
USINT	0 to 255	Error counter (8-bit)
UINT	0 to 65535	Error counter (16-bit)

4.3.3 Number of X2X sequence violations

Name:
ProtocolSequenceViolation

This register contains an error counter that specifies the number of X2X sequence violations. In the I/O configuration, parameter "Network information" can be used to help configure a data point with a bit width of 8 or 16 bits in the I/O mapping.

Data type	Values	Information
USINT	0 to 255	Error counter (8-bit)
UINT	0 to 65535	Error counter (16-bit)

4.3.4 System clock counter for checking the validity of the data frame

Name:
SDCLifeCount

Counter that is incremented with each system timer cycle. "SDC information" in the Automation Studio I/O configuration can be used to enable this register in the I/O mapping as data point "SDCLifeCount".

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Values
SINT	-128 to 127

4.4 Error handling

4.4.1 Error status - Output data

Name:
OutputControlError
OutputCopyError

This register indicates data output errors.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	OutputControlError	0	No error
		1	The module did not receive new data in time while in the mode "Output control mode = single", meaning that a bit that has already been output would have been output again by the output control buffer.
5	OutputCopyError	0	No error
		1	Oversampling output data could not be copied to the output control buffer (attempted to write to an address outside the oversampling output window, for example).
6 - 7	Reserved	-	

4.4.2 Error messages - Edge generator

Name:
EdgeGen01Error to EdgeGen04Error
EdgeGen01Warning to EdgeGen04Warning

This register indicates edge detection errors.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	EdgeGen01Error	0	No error
		1	Unit 1 error[1)]
1	EdgeGen01Warning	0	No error
		1	Unit 1 warning[2)]
2	EdgeGen02Error	0	No error
		1	Unit 2 error[1)]
3	EdgeGen02Warning	0	No error
		1	Unit 2 warning[2)]
4	EdgeGen03Error	0	No error
		1	Unit 3 error[1)]
5	EdgeGen03Warning	0	No error
		1	Unit 3 warning[2)]
6	EdgeGen04Error	0	No error
		1	Unit 4 error[1)]
7	EdgeGen04Warning	0	No error
		1	Unit 4 warning[2)]

1) **Possible errors**

- Due to "EdgeGenPollCycle", one or more timestamps from the edge generator of a unit were not able to be processed in time, and it was not possible to catch back up (see register "CfO_EdgeGenUnitPickupDiff" on page 35).
- A branched ring-shaped chain of edges in a unit is attempting to set the timestamp for an edge even though the FIFO buffer of the configured physical channel is already full (see register "CfO_EdgeGenUnitConfigEdge" on page 36 → Ring-shaped chain of edges).

2) Due to "EdgeGenPollCycle", one or more timestamps from the edge generator of a unit were not able to be processed in time, and it was possible to catch back up (see register "CfO_EdgeGenUnitPickupDiff" on page 35).

4.4.3 Error status - Overcurrent of a PWM output

Name:
DigitalOutput01Err to DigitalOutput04Err

A set bit reports an overcurrent error from the PWM hardware and disables the output until acknowledged by the user.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	DigitalOutput01Err	0	No change
		1	Overcurrent
...		...	
3	DigitalOutput04Err	0	No change
		1	Overcurrent
4 - 7	Reserved	-	

4.4.4 Acknowledge error messages - Output data

Name:
QuitOutputControlError
QuitOutputCopyError

Error messages from the "Error status - Output data" on page 25 register can be acknowledged by setting the corresponding bits in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	QuitOutputControlError	0	No change
		1	Acknowledge error
5	QuitOutputCopyError	0	No change
		1	Acknowledge error
6 - 7	Reserved	-	

4.4.5 Acknowledge error messages - Edge generator

Name:
QuitEdgeGen01Error to QuitEdgeGen04Error
QuitEdgeGen01Warning to QuitEdgeGen04Warning

The error message from register "Error messages - Edge generator" on page 25 can be acknowledged in this register by setting the respective bit.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	QuitEdgeGen01Error	0	No change
		1	Acknowledge error
1	QuitEdgeGen01Warning	0	No change
		1	Acknowledge warning
2	QuitEdgeGen02Error	0	No change
		1	Acknowledge error
3	QuitEdgeGen02Warning	0	No change
		1	Acknowledge warning
4	QuitEdgeGen03Error	0	No change
		1	Acknowledge error
5	QuitEdgeGen03Warning	0	No change
		1	Acknowledge warning
6	QuitEdgeGen04Error	0	No change
		1	Acknowledge error
7	QuitEdgeGen04Warning	0	No change
		1	Acknowledge warning

4.4.6 Acknowledge error messages - Overcurrent of a PWM output

Name:
DigitalOutput01ErrQuit to DigitalOutput04ErrQuit

Error messages from the "Error status - Overcurrent of a PWM output" on page 26 register can be acknowledged by setting the corresponding bits in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	DigitalOutput01ErrQuit	0	No change
		1	Acknowledging errors
...		...	
3	DigitalOutput04ErrQuit	0	No change
		1	Acknowledging errors
4 - 7	Reserved	-	

4.5 System timer

The module's individual functions all depend on a system timer.

4.5.1 Setting the cycle time of the system timer

Name:
CfO_SystemCycleTime
"Cycle time" in the Automation Studio I/O configuration.

The cycle time of the system timer can be set in steps of 1/8 µs in this register. The value entered in the Automation Studio I/O configuration is automatically multiplied by 8.

Information:

A setting <50 µs has a negative effect on the minimum X2X cycle time!

Data type	Values	Information
UINT	200 to 2047	System timer cycle time in steps of 1/8 µs (25 to 255.875 µs)

4.5.2 Offsetting the synchronization moment of the system cycle

Name:
CfO_SystemCycleOffset
"Cycle offset" in the Automation Studio I/O configuration.

The synchronization moment for the system cycle can be offset in steps of 1/8 µs in this register. The value entered in the Automation Studio I/O configuration is automatically multiplied by 8.

Data type	Values	Information
INT	-32768 to 32767	Cycle offset in steps of 1/8 µs (-4096 to 4095.875 µs)

4.5.3 Configuration of the cycle prescaler

Name:
CfO_SystemCyclePrescaler
"Cycle prescaler" in the Automation Studio I/O configuration.

The prescaler for setting the prescaled system timer can be configured in this register. The cycle time of the specified system timer is a product of the system timer multiple set in this register.

Data type	Values	Information
UINT	2 to 128	Multiple of the system timer

4.6 Direct I/O

"Direct I/O" makes it possible to use the physical I/Os like normal I/Os.

4.6.1 Direct operation of the output channel - Reset

Name:
CfO_DirectIOClearMask0_3
"Direct operation of output channel 01" to "Direct operation of output channel 04" in the Automation Studio I/O configuration.

If the bit for the respective channel is set in this register, then the output is reset as soon as its direct I/O output channel is reset (register "DigitalOutput0x" on page 29 in the Automation Studio I/O mapping).

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Output channel 1	0	No change
		1	Reset channel
...		...	
3	Output channel 4	0	No change
		1	Reset channel
4 - 7	Reserved	-	

4.6.2 Direct operation of the output channel - Set

Name:
CfO_DirectIOSetMask0_3
"Direct operation of output channel 01" to "Direct operation of output channel 04" in the Automation Studio I/O configuration.

If the bit for the respective channel is set in this register, then the output is set as soon as its direct I/O output channel is set (register "DigitalOutput0x" on page 29 in the Automation Studio I/O mapping).

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Output channel 1	0	No change
		1	Set channel
...		...	
3	Output channel 4	0	No change
		1	Set channel
4 - 7	Reserved	-	

4.6.3 Direct operation of the output channel - Moment of data output

Name:
CfO_OutputUpdateCycle

The moment when data is output is set with this register.

Data type	Values	Information
USINT	10	X2X cycle optimized (jitter-free)
	15	Fast reaction (with jitter)

4.6.4 Direct operation of the output channel - Output status

Name:
DigitalOutput01 to DigitalOutput04

This register contains the bits for controlling the direct I/O output channels. Depending on the configuration of registers "CfO_DirectIOClearMask0_3" on page 28 and "CfO_DirectIOSetMask0_3" on page 28, the digital outputs are set to the status of the respective bit in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	DigitalOutput01	0 or 1	Output status of channel 1
...		...	
3	DigitalOutput04	0 or 1	Output status of channel 4
4 - 7	Reserved	-	

4.6.5 Direct operation of the output channel - Enabling the PWM function

Name:
DigitalOutput01Enable to DigitalOutput04Enable

A set bit enables the PWM function.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Output channel 1	0	PWM disabled
		1	PWM enabled
...		...	
3	Output channel 4	0	PWM disabled
		1	PWM enabled
4 - 7	Reserved	-	

4.6.6 Direct operation of the output channel - Period duration

Name:
PwmPeriode01 to PwmPeriode04

The period duration can be set from 20 to 1000 µs in this register.

Data type	Values	Information
UINT	20 to 1000	The period duration is specified in microseconds.

4.6.7 Direct operation of the output channel - Pulse width

Name:
PwmDuty01 to PwmDuty04

The PWM pulse width is specified in 0.1% increments of the period duration in this register. At the beginning of each period, the output is switched on for the time set as a percentage in this register as long as the output status (register "DigitalOutput0x" on page 29) and the enable signal of the PWM function (register "DigitalOutput0xEnable" on page 29) are set.

For a detailed description of the pulse width, see "PWM" on page 11.

Data type	Values	Information
UINT	0	Output static off
	1 to 999	Corresponds to 0.1 to 99.9% of the period duration
	1000	Output static on

4.7 Oversampled I/O

4.7.1 Configuration of the output control buffer

Name:
CfO_OversampleMode
"Output mode" in the Automation Studio I/O configuration
"Output control mode" in the Automation Studio I/O configuration

The output control buffer can be configured globally for all channels in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Addressing the output control buffer	0	Absolute addressing of the output control buffer
		1	Relative addressing of the output control buffer
1	Cyclic output control	0	Single - Output control buffer entry is marked invalid after execution.
		1	Continuous - Output control buffer entry is not changed.
2 - 7	Reserved	-	

4.7.2 Configuration of the source for the sample cycle

Name:
CfO_OversampleSampleCycleID
"Sample cycle" in the Automation Studio I/O configuration.

The source for the sample cycle is configured in this register. For details, see "Reference cycle" on page 9.

Data type	Value	Information
USINT	2	System timer The value configured in the "CfO_SystemCycleTime" on page 27 register is used as the sample cycle.
	3	Prescaled system timer The "prescaled system timer" is used as sample cycle.
	10	AOAI The sample cycle is clocked with the AOAI interrupt of the X2X cycle.
	14	SOSI The sample cycle is clocked with the SOSI interrupt of the X2X cycle.

4.7.3 Configuration of the source for the user interface reference cycle

Name:
CfO_OversampleRelativeCycleID
"Reference cycle" in the Automation Studio I/O configuration.

The source for the user interface reference cycle is configured in this register. For details, see "Reference cycle" on page 9.

Data type	Value	Information
USINT	2	System timer
	3	Prescaled system timer
	10	AOAI
	14	SOSI

4.7.4 Defining the moment for copying the data to the output control buffer

Name:
CfO_OversampleConsumeCycleID
"Output copy cycle" in the Automation Studio I/O configuration.

At the time of the output copy cycle, data is copied from the "OversampleOutput0NSample" on page 32 registers into the output control buffer. For details, see "Oversampled I/O" on page 11.

Data type	Values	Information
USINT	10	X2X cycle optimized The output data is copied to the output control buffer with the AOAI interrupt of the X2X cycle.
	15	Fast reaction The output data is copied to the output control buffer immediately after being received.

4.7.5 Number of output bits to be transferred

Name:
CfO_OversampleOutputBits
"User interface size" in the Automation Studio I/O configuration.

Specifies how many bits are transferred from the "OversampleOutput0NSample" on page 32 registers to the output control buffers at the output copy cycle moment.

Data type	Values	Information
USINT	1 to 64	Output bits

4.7.6 Write area in the output control buffer

Name:
CfO_OversampleOutputWindow
"Output control mode" in the Automation Studio I/O configuration.

Defines the area in the output control buffer to which data is permitted to be written. The window is always offset relative to the current sample position. For example, a value of 128 means that the 128 bits following the current sample cycle can be written. An OutputCopyError is triggered if an attempt is made to write output sample data to a location outside of this window.
In Automation Studio, the value for this register is set to 128 bits with "Output control mode = Single" and to 255 bits with "Output control mode = Continuous".

Data type	Value	Information
USINT	0 to 255	Output window

4.7.7 Configuration of the outputs of the oversampling channels

Name:
CfO_OversampleConfigOutput
"Oversample I/O 01 → Output" to "Oversample I/O 04 → Output" in the Automation Studio I/O configuration
"Oversample I/O 01 → Output control" to "Oversample I/O 04 → Output control" in the Automation Studio I/O configuration
"Oversample I/O 01 → Output default state" to "Oversample I/O 04 → Output default state" in the Automation Studio I/O configuration

This register helps configure the outputs of the individual oversample channels.

The "Output default state" bits determine which level the respective output assumes before oversampling is started. Furthermore, the output is set to the defined "Output default state" in the event of an error.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Number of the physical output channel	0	Output channel 1
		1	Output channel 2
		2	Output channel 3
		3	Output channel 4
2 - 3	Reserved	-	
4 - 5	Output operation	1	Output can be reset by the oversample channel.
		2	Output can be set by the oversample channel.
		3	Output can be set and cleared by the oversample channel.
6 - 7	Default value output	0	Last value
		1	Output cleared by default
		2	Output set by default

4.7.8 Oversampling configuration

Name:
OversampleEnable
OversampleOutputValidate

The oversampling and copy process for the output buffer can be configured in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	OversampleEnable	0	Disables oversampling (with the next reference cycle)
		1	Enables oversampling (with the next reference cycle)
1	OversampleOutputValidate	0	Disable the copy procedure to the output control buffer.
		1	Enables the copy procedure to the output control buffer. • Used to synchronize the oversampling procedure at startup. • This makes it possible to prevent new data from being transferred to the "OversampleOutput0NSample" on page 32 registers in each X2X cycle.
2 - 7	Reserved	-	

4.7.9 Address of the new output sampling data in the output control buffer

Name:
OversampleOutputCycle

When absolute addressing of the output control buffer is being used, this register specifies the address from which the new output sample data should be copied to the output control buffer.

Data type	Values	Information
USINT	0 to 255	Address of the output control buffer

4.7.10 Offset of new output sample data

Name:
OversampleSampleOffset

When relative addressing of the output control buffer is being used, this register serves as the offset for the new output sample data. Sample address at the time of the reference cycle + Offset = address to which the new output sample data is copied in the output control buffer).

Data type	Value	Information
USINT	0 to 255	Offset of output sample data

4.7.11 Oversample output sample data

Name:
OversampleOutput01Sample1_8 to OversampleOutput04Sample1_8
OversampleOutput01Sample9_16 to OversampleOutput04Sample9_16
OversampleOutput01Sample17_24 to OversampleOutput04Sample17_24
OversampleOutput01Sample25_32 to OversampleOutput04Sample25_32
OversampleOutput01Sample33_40 to OversampleOutput04Sample33_40
OversampleOutput01Sample41_48 to OversampleOutput04Sample41_48
OversampleOutput01Sample49_56 to OversampleOutput04Sample49_56
OversampleOutput01Sample57_64 to OversampleOutput04Sample57_64

Contains the oversample output sample data. For details, see "Output data" on page 11.

Data type	Values	Information
USINT	0 to 255	Output sample data

4.7.12 Input status buffer address of the input sample data

Name:
OversampleInputCycle

The value in this register can be used to reference absolute addressing of the output control buffer.

Data type	Value	Information
USINT	0 to 255	Input status buffer address

4.8 PWM

4.8.1 Period duration

Name:
CfO_PWM01_Periode to CfO_PWM04_Periode

This register can be used to set the period duration between 20 and 1000 µs.

Data type	Value	Information
UINT	20 to 1000	The period duration is specified in µs.

4.8.2 Excitation current

Name:
CfO_PWM01_Duty1 to CfO_PWM04_Duty1

This value is enabled from the time the output is switched on until the configured excitation time expires.

Data type	Value	Information
UINT	0	Output statically off
	1000	Output statically on

4.8.3 Holding current

Name:
CfO_PWM01_Duty2 to CfO_PWM04_Duty2

This value is enabled if the output is switched on and the configured excitation time is expired.

Data type	Value	Information
UINT	0	Output statically off
	1000	Output statically on

4.8.4 Excitation time

Name:
CfO_PWM01_Duty1Time to CfO_PWM04_Duty1Time

The excitation time is set in increments according to the Excitation time base in this register.

Data type	Value	Information
UINT	0 to 65000	Definition of the excitation time in steps according to the time base

4.8.5 Excitation time base

Name:
CfO_PWM01_Duty1TimeBase to CfO_PWM04_Duty1TimeBase

The time base for the Excitation time is set in this register.

Data type	Value	Information
UINT	0 to 1000	The time base for the excitation time is specified in µs.

4.8.6 High-speed cutoff

Name:
CfO_PWM01_FastSwitchOff to CfO_PWM04_FastSwitchOff

By setting this register, the high-speed cutoff can be enabled/disabled after the output is switched off. For details, see "PWM control" on page 14.

Data type	Value	Information
UINT	0	High-speed cutoff disabled
	1	High-speed cutoff enabled

4.8.7 PWM update timestamp

Name:
CfO_PWM_UpdateCycle

This register sets the time of data output.

Data type	Value	Information
USINT	10	X2X cycle optimized (no jitter)
	15	Fast reaction (with jitter)

4.9 Edge generator

The edge generator is based on 4 units. The units are able to generate edges independently of the X2X cycle.

4.9.1 Defining the generation cycle

Name:
CfO_EdgeGenPollCycleEventID
"Generation cycle" in the Automation Studio I/O configuration.

Data type	Value	Information
USINT	2	System timer
	3	Prescaled system timer

4.9.2 Moment when output data is applied for edge generation

Name:
CfO_EdgeGenConsumeCycleEventID

This register determines when the output data for edge generation is applied within the X2X cycle.

Data type	Value	Information
USINT	10	"X2X cycle optimized" The data is force-applied between the periods ASYNC IN (AI) and ASYNC OUT (AO).
	15	"Fast reaction (with jitter)" The data is applied immediately after SYNC OUT (SO) processing.

4.9.3 Configuration of units

Name:
CfO_EdgeGenUnit01Mode to CfO_EdgeGenUnit04Mode
"Time base" in the Automation Studio I/O configuration
"Timestamp format" in the Automation Studio I/O configuration.
"Offset format" in the Automation Studio I/O configuration.
"Unit 01" to "Unit 04" in the Automation Studio I/O configuration

These registers contain the configuration bits for the respective units.

For additional information about NetTime and timestamps, see "NetTime Technology" on page 18.

When using the NetTime with 1/8 µs resolution, the synchronization jitter affects the output results (see "Synchronization jitter" on page 10).

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Resolution of the timestamp	0	1 µs
		1	1/8 µs
1	Number of bits in the timestamp register	0	16-bit
		1	32-bit
2	Offset resolution	0	1 µs
		1	1/8 µs
3	Number of bits in the offset register	0	16-bit
		1	32-bit
4	Time base	0	NetTime
5 - 6	Reserved	-	
7	Enabling/Disabling of units	0	Disabled
		1	Enabled

4.9.4 Number of timestamps for FIFO

Name:
CfO_EdgeGenUnit01TimestampFifoLim to CfO_EdgeGenUnit04TimestampFifoLim

These registers are used to define how many timestamps can be transferred to the buffer (FIFO) of a unit.

For additional information about NetTime and timestamps, see "NetTime Technology" on page 18.

For additional information, see "Using timestamps" on page 16.

Data type	Value	Information
USINT	1 to 12	FIFO limit

4.9.5 Number of timestamps per X2X cycle

Name:
CfO_EdgeGenUnit01TimestampRegCount to CfO_EdgeGenUnit04TimestampRegCount
"Timestamp elements" in the Automation Studio I/O configuration.

This register determines how many timestamps can be transferred per X2X cycle.

For additional information about NetTime and timestamps, see "NetTime Technology" on page 18.

Data type	Value	Information
USINT	1 to 4	Number of timestamps per X2X cycle

4.9.6 Pickup difference to be regained for timestamps

Name:
CfO_EdgeGenUnit01PickupDiff to CfO_EdgeGenUnit04PickupDiff

These registers are used to define how far in the past timestamps are permitted to be so that they are still caught up.

For additional information about NetTime and timestamps, see "NetTime Technology" on page 18.

For additional information, see "Using timestamps" on page 16.

In Automation Studio, if "Timestamp format = 16-bit" this register is initialized with 65535 (0xFFFF), and if "Timestamp format = 32-bit" it is initialized with 134,217,728 (0x8000000).

Data type	Value	Information
UDINT	0 to 65535	Difference to be regained in µs when "Offset format = 16-bit"
	0 to 134,217,728	Difference to be regained in µs when "Offset format = 32-bit"

4.9.7 Configuration of edge properties for each unit

Name:
CfO_EdgeGenUnit01ConfigEdge0 to CfO_EdgeGenUnit04ConfigEdge0
CfO_EdgeGenUnit01ConfigEdge1 to CfO_EdgeGenUnit04ConfigEdge1
CfO_EdgeGenUnit01ConfigEdge2 to CfO_EdgeGenUnit04ConfigEdge2
CfO_EdgeGenUnit01ConfigEdge3 to CfO_EdgeGenUnit04ConfigEdge3
"Unit 01→ Edge" to "Unit 04→ Edge" in the Automation Studio I/O configuration.
"Unit 01 → Operating mode" to "Unit 04 → Operating mode" in the Automation Studio I/O configuration.
"Unit 01 → Offset" to "Unit 04 → Offset" in the Automation Studio I/O configuration.
"Unit 01 → Unit 01" to "Unit 04 → Unit 01" in the Automation Studio I/O configuration.

The property of each of the 4 edges of a unit can be configured in these registers.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 4	Physical edge	0	Rising edge on channel 1
		1	Rising edge on channel 2
		2	Rising edge on channel 3
		3	Rising edge on channel 4
		16	Falling edge on channel 1
		17	Falling edge on channel 2
		18	Falling edge on channel 3
		19	Falling edge on channel 4
5 - 7	Reserved	-	
8 - 10	Timestamp of FIFO source	0	User interface, absolute
		1 to 3	Reserved
		4	Edge 1, relative
		5	Edge 2, relative
		6	Edge 3, relative
		7	Edge 4, relative
11	Ring-shaped chain	0	Disabled
	Default in Automation Studio for "Edge 01 = 1", "Edge 02 = 0", "Edge 03 = 0", "Edge 04 = 0"	1	Enabled
12 - 13	Offset register numbers	0	Offset register 0
		1	Offset register 1
		2	Offset register 2
		3	Offset register 3
14	Reserved	-	
15	Switching edge on/off	0	Disabled
		1	Enabled

4.9.8 Enabling units

Name:
EdgeGen01Enable to EdgeGen04Enable
EdgeGen01EnableReadback to EdgeGen04EnableReadback
"Unit 01" to "Unit 04" in the Automation Studio I/O configuration

The different units of the edge generator can be enabled/disabled using this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	EdgeGen0NEnable EdgeGen0NEnableReadback	0	Disabled
		1	Enabled
1 - 7	Reserved	-	

4.9.9 Sequence number for generating switching edges

Name:
EdgeGen01Sequence to EdgeGen04Sequence

If new timestamp data should be applied to the module, then the sequence number must be increased by the number of timestamp elements to be applied. Data from EdgeGenTimestamp arrives in the FIFO buffer first; data from "EdgeGenTimestamp1" arrives last.

For additional information, see "Using timestamps" on page 16.

Data type	Value	Information
SINT	-128 to 127	Sequence number for generating switching edges

4.9.10 Last sequence number applied by the module for edge generation.

Name:
EdgeGen01SequenceReadback to EdgeGen04SequenceReadback

The sequence number is read back in this register. Like register "EdgeGenSequence" on page 37, this register is incremented if the specified timestamps can also be recorded by the module.

Data type	Value	Information
SINT	-128 to 127	Last sequence number accepted by the module for edge generation.

4.9.11 Offset formats

There are 3 parameters available in Automation Studio for setting the offset.

4.9.11.1 Offset per unit - Transferred once during configuration

Name:
EdgeGen01Offset1 to EdgeGen04Offset1
...
EdgeGen01Offset4 to EdgeGen04Offset4
"Offset 01 value" to "Offset 04 value" in the Automation Studio I/O configuration

The 4 offsets of an edge generator unit are written in this register. Depending on the configuration in register "Edge generator unit mode" on page 34, the offset values are handled in µs or 1/8 µs steps.

For information regarding how to use the register and set the offset formats in Automation Studio, see "Offset formats" on page 16.

Data type	Value	Information
UINT	0 to 65535	16-bit offset
UDINT	0 to 134,217,728	Offset when "Offset format = 32-bit" and "Time base" = 1 µs
	0 to 1,073,741,824	Offset when "Offset format = 32-bit" and "Time base" = 1/8 µs

4.9.11.2 Offset per unit - Acyclic transfer

Name:
CfO_EdgeGen01Offset_32bit1 to CfO_EdgeGen04Offset_32bit1
...
CfO_EdgeGen01Offset_32bit4 to CfO_EdgeGen04Offset_32bit4

The 4 offsets of an edge generator unit can be written acyclically using these registers. Depending on the configuration in register "Edge generator unit mode" on page 34, the offset values are handled in µs or 1/8 µs steps.

For information regarding how to use the register and set the offset formats in Automation Studio, see "Offset formats" on page 16.

Data type	Value	Information
UDINT	0 to 134,217,728	Offset when "Offset format = 32-bit" and "Time base" = 1 µs
	0 to 1,073,741,824	Offset when "Offset format = 32-bit" and "Time base" = 1/8 µs

4.9.12 Timestamp registers

Name:
EdgeGen01Timestamp1 to EdgeGen04Timestamp1
...
EdgeGen01Timestamp4 to EdgeGen04Timestamp4

Register for the timestamps to which the edges to be generated are referenced.

For additional information about NetTime and timestamps, see "NetTime Technology" on page 18.

For additional information, see "Using timestamps" on page 16.

Data type	Values
INT	-32768 to 32767
DINT	-2147483648 to 2147483647

4.10 Minimum X2X cycle time

The minimum X2X cycle time is strongly dependent on the configured functions and the resulting load on the module. Setting "Fast reaction" and a very short system cycle (<50 µs) generally have a negative effect on the minimum X2X cycle time. This can result in error behavior with short X2X cycle times.